RCL Semiconductors Ltd.

HC245 Octal Bus Transceivers with 3-State Outputs

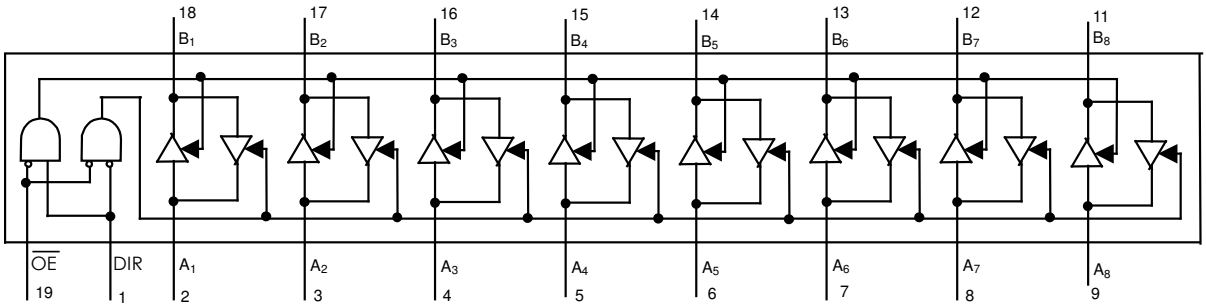
GENERAL DESCRIPTION

The Octal Bus Transceivers are designed for asynchronous bi-direction communication between data buses. The control-function implementation minimizes external timing requirements. The devices allow data transmission from bus A to bus B or from bus B to bus A, depending on the logic level at the direction-control input (DIR). The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

FEATURES

Octal bi-direction bus interface
Non-inverting 3-state outputs
Output capability: bus driver

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

Truth Table

INPUTS		INPUTS / OUTPUTS	
$\overline{OE}$	DIR	An	Bn
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

Note: H = High Level L = Low Level X = don't care Z = High impedance off state.

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
DC supply voltage (V_{DD})	- 0.5 ~ + 7.0	V
Input clamp current (I_{IK}) Vi<0 or Vi> V_{DD} (see Note)	±20	mA
Output clamp current (Iok) Vo<0 or Vo> V_{DD} (see Note)	±20	mA
Continuous output current (Io) Vo=0 to V_{DD}	±35	mA
Continuous current through V_{DD} or Vss	±70	mA
Storage Temperature (TSTG)	-65 ~ +150	℃

Note: The input and output voltage rating may be exceeded if the input and output current rating are observed.

RECOMMENDED OPERATING CONDITIONS

Parameter		54HC245			74HC245			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{DD} Supply Voltage		2	5	6	2	5	6	V
V_{IH} High Level Input Voltage	V_{DD} = 2.0 V	1.5			1.5			V
	V_{DD} = 4.5 V	3.15			3.15			
	V_{DD} = 6.0 V	4.2			4.2			
V_{IL} Low Level Input Voltage	V_{DD} = 2.0 V	0		0.5	0		0.5	V
	V_{DD} = 4.5 V	0		1.35	0		1.35	
	V_{DD} = 6.0 V	0		1.8	0		1.8	
V_I Input voltage		0		V_{DD}	0		V_{DD}	V
Vo Output voltage		0		V_{DD}	0		V_{DD}	V
tt Input Transition time (rise and fall)	V_{DD} = 2.0 V	0		1000	0		1000	ns
	V_{DD} = 4.5 V	0		500	0		500	
	V_{DD} = 6.0 V	0		400	0		400	
T_A Operating Temperature		-55		125	-40		85	℃

DC ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions		VDD	T_A = 25℃			54HC245		74HC245		Unit
					Min.	Typ	Max.	Min.	Max.	Min.	Max.	
V_{OH}		V_I = V_{IH} or V_{IL}	I_{OH} = -20uA	2.0 V	1.9	1.998		1.9		1.9		V
				4.5 V	4.4	4.499		4.4		4.4		
				6.0 V	5.9	5.999		5.9		5.9		
			I_{OH} = -6mA	4.5 V	3.98	4.3		3.7		3.84		
			I_{OH} = -7.8mA	6.0 V	5.48	5.8		5.2		5.34		
V_{OL}		V_I = V_{IH} or V_{IL}	I_{OL} =20uA	2.0 V		0.002	0.1		0.1		0.1	V
				4.5 V		0.001	0.1		0.1		0.1	
				6.0 V		0.001	0.1		0.1		0.1	
			I_{OL} = 6mA	4.5 V		0.17	0.26		0.4		0.33	
			I_{OL} =7.8mA	6.0 V		0.15	0.26		0.4		0.33	
I_I	DIR or $\overline{OE}$	V_I = V_{DD} or 0		6.0 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	V_O = V_{DD} or 0		6.0 V		±0.01	±0.5		±10		±5	uA
Icc		V_I = V_{DD} or 0 I_O = 0		6.0 V			8		160		80	uA
Ci	DIR or $\overline{OE}$			2V ~ 6V		3	10		10		10	pF

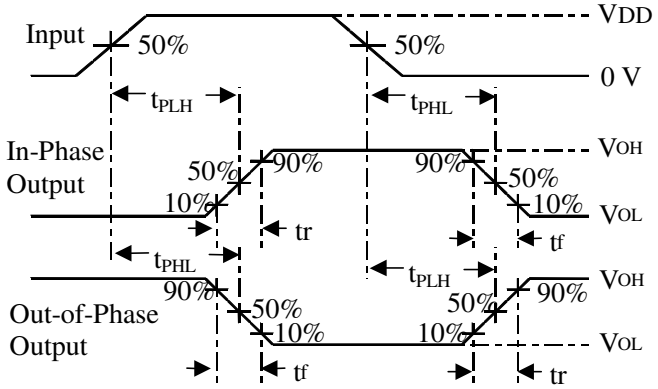
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, unless otherwise noted)(see Figure 1)

Parameter	From (Input)	To (Output)	V_{DD}	T_A = 25℃			54HC245		74HC245		Unit
				Min	Typ	Max	Min	Max	Min	Max	
tpd	A or B	B or A	2.0 V		40	105		160		130	ns
			4.5V		15	21		32		26	
			6.0 V		12	18		27		22	
ten	$\overline{OE}$	A or B	2.0 V		125	230		340		290	ns
			4.5V		23	46		68		58	
			6.0 V		20	39		58		49	
tdis	$\overline{OE}$	A or B	2.0 V		74	200		300		250	ns
			4.5V		25	40		60		50	
			6.0 V		21	34		51		43	
t_t		A or B	2.0 V		20	60		90		75	ns
			4.5V		8	12		18		15	
			6.0 V		6	10		15		13	

AC ELECTRICAL CHARACTERISTICS (C_L=150pF, unless otherwise noted)(see Figure 1)

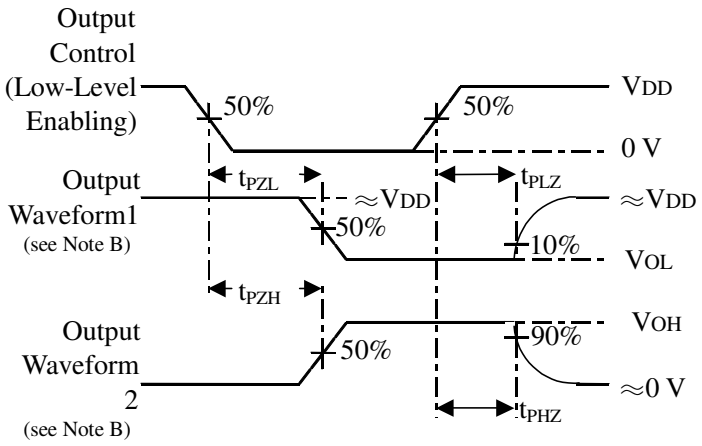
Parameter	From (Input)	To (Output)	V_{DD}	T_A = 25℃			54HC245		74HC245		Unit
				Min	Typ	Max	Min	Max	Min	Max	
tpd	A or B	B or A	2.0 V		54	135		200		170	ns
			4.5V		18	27		40		34	
			6.0 V		15	23		34		29	
ten	$\overline{OE}$	A or B	2.0 V		150	270		405		335	ns
			4.5V		31	54		81		67	
			6.0 V		25	46		69		56	
t_t		A or B	2.0 V		45	210		315		265	ns
			4.5V		17	42		63		53	
			6.0 V		13	36		53		45	

AC SWITCHING WAVEFORM AND AC TEST CIRCUIT

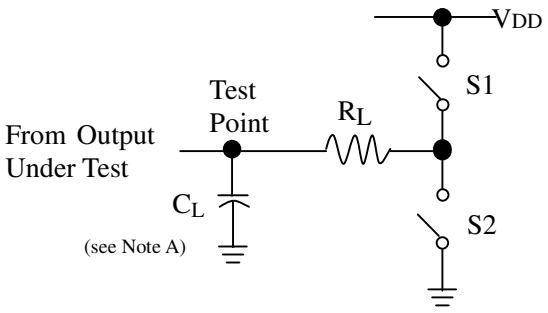


Voltage Waveforms
Propagation Delay and Output Transition Times

Voltage Waveform
Input Rise and Fall Times



Voltage Waveforms
Enable and Disable Times for 3-state Outputs



Parameter		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1k Ω	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1k Ω	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		-	50 pF or 150 pF	Open	Open

Notes:
A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:
PRR≤ 1 MHz, Zo = 50 Ω, t_r=6ns, t_f =6ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

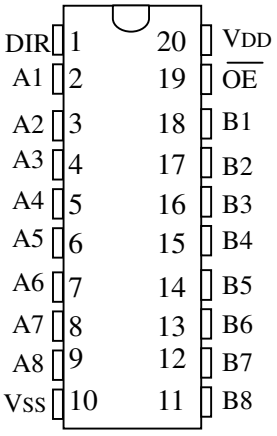
Figure 1. Load Circuit and Voltage Waveforms

OPERATING CHARACTERISTICS (T_A = 25℃)

Parameter	Test Condition	Typ	Unit
C_{pd} Power dissipation capacitance per transceiver	No load	40	pF

Note : C_{PD} determines the no load dynamic power consumption (P_D in μ w) :
$P_D=C_{PD} V_{DD}^2 fi + Icc V_{DD}$,
and the no load dynamic current consumption, $Is = C_{PD} V_{DD} f + Icc$.

PIN DESCRIPTION



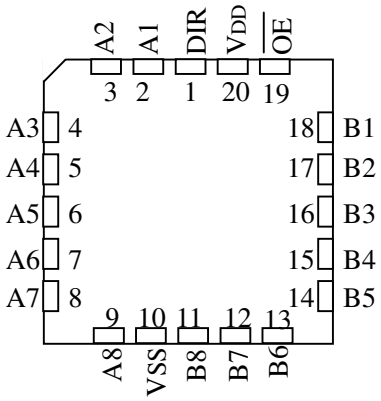


Fig.2 Pin Configuration

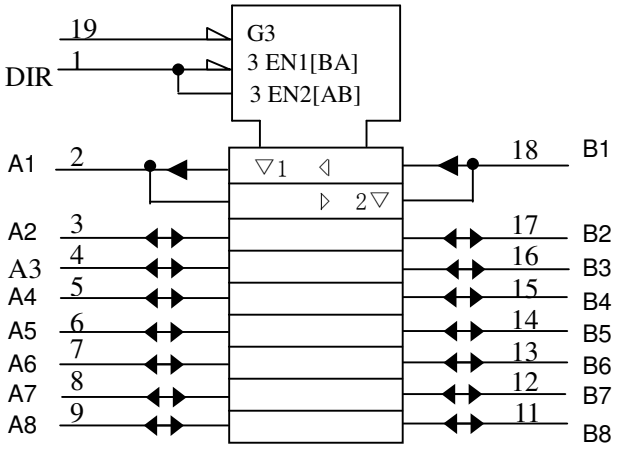
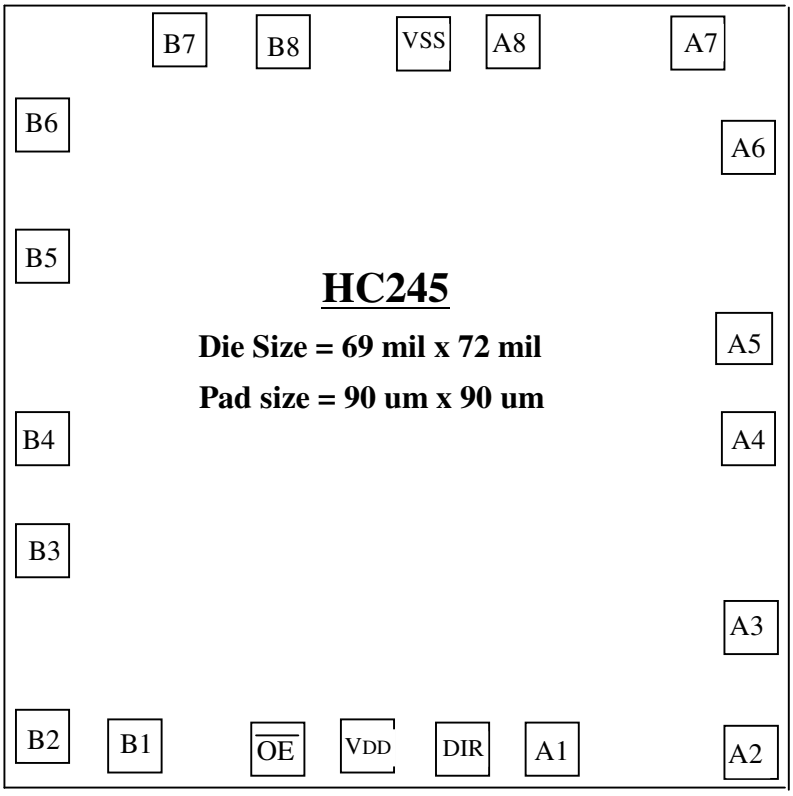


Fig.3 IEC Logic Symbol

PIN NO.	SYMBOL	DESCRIPTION
1	DIR	Direction control
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs / Outputs
10	VSS	Ground (0V)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs / Outputs
19	$\overline{OE}$	Output enable input (active Low)
20	VDD	Positive power supply

PAD DIAGRAM



The Coordinate of Low Left Corner for Each Pad

B2 (-741.9, -722.4)	A3 (651.8, -503.2)	B8 (-267.8, 657.6)
$\overline{B1}$ (-558.3, -747.1)	A4 (651.8, -124.2)	B7 (-466.6, 657.6)
$\overline{OE}$ (-288.0, -747.1)	A5 (651.8, 74.6)	B6 (-741.9, 506.6)
VDD(-111.4, -742.5)	A6 (651.8, 454.0)	B5 (-741.9, 236.8)
DIR (85.8, -747.1)	A7 (559.5, 657.6)	B4 (-741.9, -143.4)
A1 (262.6, -747.1)	A8 (179.3, 657.6)	B3 (-741.9, -342.2)
A2 (642.8, -747.1)	VSS (2.7, 658.6)	